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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/611,037	07/06/2000	Andras Kuthi	LAMIP077A	5329

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EXAMINER

ALEJANDRO MULERO, LUZ L

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/611,037

Applicant(s)

KUTHI ET AL.

Examiner

Luz L. Alejandro

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14-21 and 33-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 14-21 and 33-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 33-35, 37-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita et al., U.S. Patent 5,593,540 in view of Admitted prior art.

Tomita et al. shows the invention substantially as claimed including in a chamber 1 for processing a semiconductor wafer W through plasma etching operations, the chamber being in an operational state and including a support chuck 61 for holding the semiconductor wafer, a RF power supply 12 for an upper electrode 3, a method of processing the wafer through plasma etching operations, comprising: striking a plasma

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in the plasma region in the chamber; and generating an increase in bias voltage/ion bombardment energy directed at a wafer surface of a semiconductor wafer W and a decrease in bias voltage directed at the top electrode 2, the top electrode 3 having a center region, a first surface, and a second surface, the first surface having an inlet 55 that is configured to receive processing gases from a source (71a,71b,71c) that is external to the chamber and facing a cooling plate 53 and flowing processing gases into the center region; the second surface facing the interior portion of the plasma chamber and having a plurality of gas feed line holes 55 that lead to a plurality of electrode openings which expose the gas to the plasma, wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface area that is proximate to the second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area (see figs. 1-4 and col. 3-line 40 to col. 5-line 60). Note that inherently the plasma sheath will form within the inlet openings 55 to form the second plasma sheath surface area since the openings have an opening diameter of 0.6mm (see applicant's specification at page 13, lines 22-24 and col. 5-lines 3-5 of Tomita et al.).

Tomita et al. fails to expressly disclose a pair of RF power sources. With respect to the dual RF power sources, admitted prior art in fig. 1A discloses a first RF power source 118b connected to a lower electrode and a second RF power source 118a connected to an upper electrode (see fig. 1A and page 1-line 24 to page 2-line 16 of

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specification). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Tomita et al. so as to include two RF power sources coupled to the upper and lower electrodes, respectively, because the Admitted prior art shows this to be a suitable structure for a plasma etching apparatus.

Claims 14-21 and 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art (APA) in view of Chang et al., U.S. Patent 4,854,263.

APA shows the invention substantially as claimed including in a chamber 102 for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck 104 for holding the wafer, a pair of RF power sources 118a/118b, and a top electrode 114, a method for processing the wafer through plasma etching operations, comprising: striking a plasma in a plasma region of the chamber; the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes/electrode openings, wherein the plurality of electrode openings are configured to define the second surface which is located over the wafer surface of the semiconductor wafer, wherein the plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first

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plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath having a second plasma sheath surface area that is proximate to the second surface (see, figs. 1A-1C of the APA and their descriptions).

The admitted prior art does not expressly disclose that the electrode openings diameter is greater than the gas feed holes diameter. Chang et al. an electrode which has been formed so as to comprise gas feed holes 33 that lead to a plurality of electrode openings 31/34, the electrode openings having diameters that are greater than gas feed hole diameters of the plurality of gas feed holes in order to enhance dissociation and reactivity of the gas(es) (see col. 5-lines 33-53 and figs. 1-3).

Therefore, in view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the APA as to comprise electrode openings having diameters that are greater than gas feed hole diameters of the plurality of gas feed openings because this would enhance dissociation and reactivity of the gas(es). Additionally, in teachings of the APA modified by Chang et al.: a) the second plasma sheath surface area will be greater than the first plasma sheath surface area (since the plasma sheath will form within the inlet openings, note that the openings diameter is more than 0.5mm, also see applicant's specification at page 13, lines 22-24 and col. 6-lines 24-26 of Chang et al.), which will generate an increase in bias voltage and ion bombardment energy directed at a wafer surface of the wafer and a decrease in bias voltage directed at the top electrode, and b) plasma sheath will shift into the electrode openings of the top electrode. Note that with respect to claims 33-40, the above first plasma sheath surface area will be the second plasma sheath surface

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area and the above second plasma sheath surface area will be the first plasma sheath surface area.

With respect to claim 15, note that the top electrode is coupled to one of the pair of RF power sources and the support chuck is coupled to the other one of the pair of RF power sources.

Concerning claims 16-17 and 20, APA and Chang do not disclose that the gas feed holes have a diameter of about 0.1mm, the electrode openings have a depth of $1/32$ to $1/4$ of an inch, and fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at about 0.5 to 5mm, but it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize through routine experimentation the gas feed hole diameter, the electrode opening depth, and the spacing of the second plasma sheath surface from the second surface depending upon, for example, the particular size of the semiconductor being processed, and therefore the claimed dimensions would not lend patentability to the claimed invention absent the showing of unexpected results.

Regarding claim 18, note that electrode 114 of APA is movable in the vertical direction and Chang et al. discloses such separation dimension. Therefore, it would have been obvious to it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the separation of the second surface and the wafer surface, as claimed, depending upon, for example, the desired plasma

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density, and therefore the claimed dimensions would not lend patentability to the claimed invention absent the showing of unexpected results. Additionally,

With respect to claim 19, note that two or more buffer plates are inserted within the center region of the top electrode (see fig. 1B).

Claims 14-21 and 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al., U.S. Patent 4,854,263 in view of Admitted prior art (APA).

Chang et al. shows the invention substantially as claimed including in a chamber 10 for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a holder for holding the wafer, a RF power, and a top electrode 11, a method for processing the wafer through plasma etching operations, comprising: striking a plasma in a plasma region of the chamber; the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes 33 that lead to a plurality of electrode openings 31/34 that have diameters greater than gas feed hole diameters, wherein the plurality of electrode openings are configured to define the second surface which is located over the wafer surface of the semiconductor wafer, wherein the plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath

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surface area that is proximate to the wafer surface and a second plasma sheath having a second plasma sheath surface area that is proximate to the second surface (see figs. 1-3, col. 4, lines 60-64, and col. 5-lines 33-53). Furthermore note that: a) the second plasma sheath surface area will be greater than the first plasma sheath surface area (since the plasma sheath will form within the inlet openings, note that the openings diameter is more than 0.5mm, also see applicant's specification at page 13, lines 22-24 and col. 6-lines 24-26 of Chang et al.), which will generate an increase in bias voltage and ion bombardment energy directed at a wafer surface of the wafer and a decrease in bias voltage directed at the top electrode, and b) plasma sheath will shift into the electrode openings of the top electrode. Note that with respect to claims 33-40, the above first plasma sheath surface area will be the second plasma sheath surface area and the above second plasma sheath surface area will be the first plasma sheath surface area.

Chang et al. does not expressly disclose holding the substrate with a chuck, the use of a pair of power sources, and inserting two or more gas buffer plates within the center region of the top electrode. APA discloses holding the wafer 106 with a chuck 104, coupling a pair of RF power sources 118a/118b to the top electrode and the chuck, and inserting two or more buffer plates within the center region of the top electrode (see, figs. 1A and 1B, and their descriptions). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Chang et al. by holding the wafer with a chuck and by coupling RF power to the chuck in order to efficiently and effectively hold the wafer during processing, in

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order to generate a bias voltage within the plasma region, and in order to evenly distribute the processing gases throughout the top electrode, respectively, thereby increasing the ion bombardment towards the substrate and improving the process being performed on the substrate.

Concerning claims 16-17 and 20, Chang et al. and APA do not disclose that the gas feed holes have a diameter of about 0.1mm, the electrode openings have a depth of 1/32 to 1/4 of an inch, and fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at about 0.5 to 5mm, but it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize through routine experimentation the gas feed hole diameter, the electrode opening depth, and the spacing of the second plasma sheath surface from the second surface depending upon, for example, the particular size of the semiconductor being processed, and therefore the claimed dimensions would not lend patentability to the claimed invention absent the showing of unexpected results.

Regarding claim 18, note that Chang et al. discloses an electrode separation within the claimed dimension range.

Response to Arguments

Applicant's arguments filed 3/7/05 have been fully considered but they are not persuasive with respect to the rejection of claims 33-35, 37-38, and 40 over Tomita et al. in view of Admitted prior art. The arguments with respect to claims 14-21, 36 and 39

over Tomita et al. in view of APA and further in view of Chang et al., are considered persuasive and therefore, the rejection has been withdrawn. However, note that a new ground of rejection has been made over claims 14-21 and 33-40.

Applicant argues that a prima facie case of inherency with respect to plasma forming in the holes of the Tomita et al. reference has not been established. However, the examiner submits that statements both in applicant's own specification and in the Tomita et al. reference establish the case of inherency. Furthermore, while the intention in the Tomita et al. reference is to suppress polymerization in the holes from the plasma, it is clear simply by the use of the word "suppressed" that while not as much plasma will be present in the holes than in the prior art due to the flow rate of the gas, some plasma will still be present (see col. 2-lines 37-53). Furthermore, and as evidenced by applicant's declaration, polymerization occurs at high plasma densities but may not necessarily occur at lower plasma densities.

Applicant argues that "The size of the electrode openings is but one parameter or feature of the presently claimed method. It is not a valid assumption to conclude that any electrode having electrode openings of a particular size (in the instant application the size is recited to be at least 0.5mm) will result in a plasma shift into the electrode openings.". However, in the declaration under 37 CFR 1.132, paragraphs 4-5, signed by inventor Lumin Li, it is clearly stated that "We specified the minimum hole size of 0.5mm. The diameter of any hole larger than 0.5mm will meet the requirement for a hole size, depending on various process parameters..." (paragraph 4) and "In order to include a wide range of plasma etch process regimes, we chose a diameter of 0.5 mm

conservatively as the minimum size for the worst case..." (paragraph 5). Therefore, one of ordinary skill in the art at the time of the invention was made would expect that an electrode opening of at least 0.5 mm (the cited reference disclose 0.6 mm and smaller than 0.8mm) is big enough to shift plasma into the opening.

Applicant argues that "Among other design features, the gas feed holes (228) are smaller than the electrode openings (202b), which allows the shift to occur while preventing plasma formation in the gas feed holes (228)". However, it should be noted that: a) claims 33-35, 37-38, and 40 do not comprise such limitation, and b) claims 14-40 are rejected under new grounds of rejection.

Regarding the declaration under 37 CFR 1.132, the examiner can appreciate that forming plasma in a gas hole of a showerhead, for example, may not be desirable but this does not take away from the fact that in Tomita et al. inherently the plasma will be shifted into the gas holes. Additionally, paragraph 2, states "To achieve a mass flow speed...the holes in the showerhead must be smaller than 0.6mm. The reference specifies 0.6mm as the maximum diameter of the hole.", however, col. 2, lines 30-34, of Tomita et al., clearly states that the holes diameter should be smaller than 0.8mm, not 0.6mm, as mistakenly stated by applicant. In paragraph 3, applicant states that "The holes in the claimed invention must big enough to allow plasma to exist inside to form a hollow cathode discharge.". However, it should be noted that in the specification, page 13, lines 22-24 and in paragraphs 4-5 of the declaration (see the above paragraphs for citations), applicant clearly states that 0.5mm is the minimum hole size that is considered big enough. Therefore, the teachings of Tomita et al., of a hole diameter of

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0.6mm or smaller than 0.8mm will meet the minimum requirement for the worst case. Also, it is noted that at the end of paragraph 5, applicant states that "For most of our applications, we prefer diameter of showerhead holes to be 2 ~ 10mm.". However, it should be notice that the application of the instant invention does not disclose such hole dimension.

Concerning the fact that in the instant invention the hole size is increased in order to intentionally introduce plasma, as stated above, in Tomita et al. the hole dimensions are very similar to those in the instant invention so one would expect that if plasma were to shift into the holes of the instant invention, it would shift into the holes of Tomita et al. whether it is desirable or undesirable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luz L. Alejandro whose telephone number is 571-272-1430. The examiner can normally be reached on Monday to Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luz L. Alejandro
Primary Examiner
Art Unit 1763

May 11, 2005